Read/Write	ADR	HEXADR	NAME	Description	OS
Read	53768	$D208	ALLPOT	Audio control	all
Write	53768	$D208	AUDCTL	Pot Port State	all

AUDCTL (Write)#

AUDCTL is the option byte which affects all sound channels. This bit assignment is:

Bit	Description
7	0=17 bit poly counter 1=9 bit polynomial noise
6	0=clock channel 1 with 64kHz 1=Clock channel one with 1.79 MHz (NTSC) or 1.77MHz (PAL)
5	0=clock channel 3 with 64kHz 1=Clock channel three with 1.79 MHz (NTSC) or 1.77MHz (PAL)
4	0=clock channel 2 with 64kHz 1=Join channels two and one (16 bit, with 2/4=MSB, 1/2=LSB)
3	0=clock channel 4 with 64kHz 1=Join channels four and three (16 bit, with 2/4=MSB, 1/2=LSB)
2	1=Insert high pass filter into channel one, clocked by channel two
1	1=Insert high pass filter into channel three, clocked by channel four
0	0=main clock base 64 KHz 1=16 KHz main clock base

ALLPOT (Read)#

Shows if the readings of the pots are (already) valid.

Bit	Paddle	Shadow	Register
0	Paddle 0	PADDL0	POT0
1	Paddle 1	PADDL1	POT1
2	Paddle 2	PADDL2	POT2
3	Paddle 3	PADDL3	POT3
4	Paddle 4	PADDL4	POT4
5	Paddle 5	PADDL5	POT5
6	Paddle 6	PADDL6	POT6
7	Paddle 7	PADDL7	POT7

If a bit equals zero (0), then the register value for that pot (e.g. Bit 0 = POT0) is valid; if the Bit is one (1), then the value is not (yet) valid, because the reading/scan is not finished yet or there is no paddle connected.

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see also: Controller topics, POTGO, ALLPOT, SKCTL

previous: AUDC4,POT7

next: STIMER,KBCODE